Remarks

Applicant appreciates the Examiner's indication that Claims 8-9 are allowable but Applicant maintains that all of the (previously-presented and new) rejections are improper and are based on clearly flawed reasoning and, therefore, should be withdrawn. At the outset, Applicant traverses each of the rejections and their underlying rationale. This traversal is based on careful study of the cited references and the Examiner's rationale as presented in this most recent Office Action. As Applicant's position on the current rejections has largely been presented in the previously-filed Response, the following discussion incorporates the previously-filed Response.

In the final Office Action dated July 14, 2008, the following rejections are presented: claims 1-2 and 5-6 stand rejected under 35 U.S.C. § 103(a) over the Moser reference (U.S. Patent No. 6,853,696) in view of the Savoj reference ("Design of Half-Rate Clock and Data Recovery Circuits for Optical Communications Systems"); claims 3-4 stand rejected under 35 U.S.C. § 103(a) over the Moser reference in view of the Savoj reference and further in view of the Morgan reference (U.S. Patent No. 6,320,406); and claim 7 stands rejected under 35 U.S.C. § 103(a) over the Moser reference in view of the Savoj reference and further in view of the Lee reference (U.S. Patent No. 5,734,301).

Applicant submits that each of the rejections is clearly erroneous because each fails to present a combination of teachings that would correspond to the claimed invention and to present any proper evidence that a skilled artisan would be motivated to combine the teachings as asserted. First, each asserted combination is based on the assertion that Moser in view of Savoj would teach the claimed invention with Applicant's claimed phase detector. At page 2 of the Office Action, the Examiner acknowledges this deficiency implicitly by attempting to argue that correspondence can be met if it can be shown that the claimed phase detector is the same as or a functional equivalent to a frequency detector. Such an argument may be applicable under certain situations of a "means plus function" analysis under 35 U.S.C. § 112, paragraph 6, but otherwise expressly violates the Examiner's requirements to interpret the claim language without ignoring limitations and in a manner that is consistent with the plain meaning in a manner consistent with Applicant's Specification. See M.P.E.P. § 2173.02 (interpreting claim

terminology in view of specification) and M.P.E.P. § 706.03(d) (plain meaning). Moreover, as M.P.E.P. §2173.05(a) indicates that the meaning of every term used in a claim should be apparent from the prior art or from the specification and drawings at the time the application is filed, it is clear that from the specification and the asserted prior art that a phase detector is different than a frequency detector.

Further, from a technical perspective, the Examiner is plainly wrong. First, a skilled artisan would not agree that (Applicant's or a generic) phase detector is the same as or a functional equivalent to a frequency detector. By definition, a frequency detector is a circuit that generates a signal which represents the difference in frequency between two signal inputs, and a phase detector is a circuit that generates a signal which represents the difference in phase between two signal inputs. As is well known and documented in the claims of hundreds of issued U.S. Patents, these types of detectors are structurally and functionally different; as this view is fully appreciated by the U.S. Patent and Trademark Office, for a small sample of such patent documents, reference may be made to U.S. Patent Nos. 7,218,157, 7,215,207, 7,190,231, 7,180,963, 7,180,376, 7,173,495, 7,158,601, and 7,154,979. Second, the Examiner is also wrong in basing this technical argument on the premise that Applicant's specification supports the position that Applicant's phase detector "only outputs frequency error"; on the contrary, Applicant's phase detector provides (in FIG. 2) a first pair of signals (PQ and PQ_) and a second pair of signals (PI and PI_) indicative of the phase difference (see, *e.g.*, published Application at paragraph 14).

As presented earlier and with no apparent response from the Examiner (see M.P.E.P. 7070.07(f)), the asserted combination of references fails to cure other noted deficiencies. In particular, Applicant finds nothing in the combination to teach or suggest a frequency detector that uses double edge clocked bi-stable circuits as asserted by the Examiner (*see* Office Action page 4). Instead, the Savoj reference (as used in the combination) discloses implementing a phase detector using double-edge-triggered flipflops (*see* Figure 11 and Section 3.2.2). The Savoj reference then discusses how a phase and frequency detector (PFD) may be constructed using two of the phase detectors (*see* Figure 12 and Section 3.2.3). As such, the references cannot be read to teach all the elements recited in Applicant's claims.

Accordingly, the asserted combination of references renders a hypothetical circuit that fails to correspond to the claimed invention.

Applicant also maintains that there is no proper reason to combine the Moser and Savoj references and that the Examiner's explanation is illogical as it would not yield an operable circuit consistent with the purpose of the Moser reference. For example, Savoj teaches using multiple phase detectors to implement a combined phase and frequency detection circuit, whereas Moser explicitly separates frequency detection from phase detection using a multiplexer that selects the output of either the frequency detector (DFD) or the phase detector (PD), but not both. Furthermore, as discussed above, Moser explicitly states that the frequency detector does not include a phase detection function. Combining these aspects would contradict the intended operation of the Moser (main) reference. As explained at M.P.E.P. § 2143.01 and with reference to the authoritative decision, *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984), a §103 rejection cannot be maintained when the asserted modification undermines purpose of main reference.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and that the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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